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Claims

[c1] Unknown;Donna Klempner;1. A method of operating a switch having ON and OFF states and having a parasitic gate capacitance, said switch comprising a pair of DMOS FETs having a shared gate terminal, the sources of said DMOS FETs being connected to each other and the drains of said DMOS FETs being connected to the input and output terminals of said switch respectively, and said shared gate terminal being connected to a drain of a programming transistor, the gate of said programming transistor receiving a gate voltage, the source of said programming transistor receiving a programming voltage, and the drains of said DMOS FETs being biased at a bias voltage level, comprising the following steps:
(a) transitioning from a first level of said programming voltage to a second level of said programming voltage, said second level of said programming voltage being lower than said first level of said programming voltage and being higher than said bias voltage level by an amount sufficient to turn on said switch; and
(b) transitioning from a first level of said programming transistor gate voltage to a second level of said programming transistor gate voltage, said first level of said

programming transistor gate voltage being approximately equal to said first level of said programming voltage, and said second level of said programming transistor gate voltage being lower than said second level of said programming voltage by an amount sufficient to turn on said programming transistor, whereby said second level of said programming voltage is applied to said shared gate terminal of said switch via said programming transistor.

[c2] 2. The method as recited in claim 1, further comprising the following steps performed after step (b):
(c) transitioning from said second level of said programming voltage back to said first level of said programming voltage;
(d) transitioning from said second level of said programming transistor gate voltage back to said first level of said programming transistor gate voltage; and
(e) applying a signal voltage level to said input terminal of said switch that is not greater than said first level of said programming voltage, while said switch is turned on.

[c3] 3. The method as recited in claim 2, further comprising the following steps:
(f) transitioning from said first level of said programming voltage to a third level of said programming voltage

lower than said second level of said programming voltage and close enough to said bias voltage level that said switch is turned off; and

(g) transitioning from said first level of said programming transistor gate voltage to a third level of said programming transistor gate voltage lower than said third level of said programming voltage by an amount sufficient to turn on said programming transistor, whereby said third level of said programming voltage is applied to said shared gate terminal of said switch via said programming transistor.

[c4] 4. The method as recited in claim 3, further comprising the following steps:

transitioning from said first level of said programming voltage to said second level of said programming voltage; and

transitioning from said first level of said programming transistor gate voltage to a fourth level of said programming transistor gate voltage close enough to said second level of said programming voltage to turn off said programming transistor.

[c5] 5. The method as recited in claim 1, further comprising the following steps performed after step (b):

(c) transitioning from said second level of said programming voltage back to said first level of said programming

voltage;

(d) transitioning from said second level of said programming transistor gate voltage back to said first level of said programming transistor gate voltage;

(e) after step (c), transitioning from said first level of said programming voltage to a third level of said programming voltage lower than said second level of said programming voltage and close enough to said bias voltage level that said switch would be turned off if said third level of said programming voltage were applied to said shared gate terminal of said switch; and

(f) after step (d), transitioning from said first level of said programming transistor gate voltage to a third level of said programming transistor gate voltage greater than said third level of said programming voltage, whereby said programming transistor is turned off.

[c6] 6. A circuit comprising:

a switch having ON and OFF states and having a parasitic gate capacitance, said switch comprising a pair of DMOS FETs having a shared gate terminal, the sources of said DMOS FETs being connected to each other and the drains of said DMOS FETs being connected to the input and output terminals of said switch respectively, and biased at a bias voltage level; and

a control circuit for turning said switch on and off, said

control circuit comprising:

a programming transistor having its drain connected to said shared gate terminal of said switch, its source connected to receive a programming voltage, and its gate connected to receive a programming transistor gate voltage;

first circuitry for causing a first transition from a first level of said programming voltage to a second level of said programming voltage, said second level of said programming voltage being lower than said first level of said programming voltage and being higher than said bias voltage level by an amount sufficient to turn on said switch; and

second circuitry for causing a second transition from a first level of said programming transistor gate voltage to a second level of said programming transistor gate voltage, said first level of said programming transistor gate voltage being approximately equal to said first level of said programming voltage, and said second level of said programming transistor gate voltage being lower than said second level of said programming voltage by an amount sufficient to turn on said programming transistor, whereby said second level of said programming voltage is applied to said shared gate terminal of said switch via said programming transistor.

[c7] 7. The circuit as recited in claim 6, wherein said programming transistor is a PMOS transistor.

[c8] 8 The circuit as recited in claim 6, wherein said second circuitry comprises floating control logic.

[c9] 9. The circuit as recited in claim 6, wherein said second circuitry comprises a level shifter.

[c10] 10. The circuit as recited in claim 6, wherein after said second transition, said first circuitry causes a third transition from said second level of said programming voltage back to said first level of said programming voltage, and said second circuitry causes a fourth transition from said second level of said programming transistor gate voltage back to said first level of said programming transistor gate voltage.

[c11] 11. The circuit as recited in claim 10, further comprising a driver circuit coupled to said input terminal of said switch, and an ultrasound transducer coupled to said output terminal of said switch and driven by said driver circuit when said switch and said driver circuit are both turned on.

[c12] 12. The circuit as recited in claim 6, further comprising a receiver coupled to said input terminal of said switch, and an ultrasound transducer coupled to said output ter-

minal of said switch, said ultrasound transducer being coupled to said receiver when said switch and said receiver are both turned on.

[c13] 13. The circuit recited in claim 10, wherein said first circuitry causes a fifth transition from said first level of said programming voltage to a third level of said programming voltage lower than said second level of said programming voltage and close enough to said bias voltage level that said switch is turned off; and said second circuitry causes a sixth transition from said first level of said programming transistor gate voltage to a third level of said programming transistor gate voltage lower than said third level of said programming voltage by an amount sufficient to turn on said programming transistor, whereby said third level of said programming voltage is applied to said shared gate terminal of said switch via said programming transistor.

[c14] 14. The circuit as recited in claim 13, wherein after said sixth transition, said first circuitry causes a seventh transition from said third level of said programming voltage back to said first level of said programming voltage, and said second circuitry causes an eighth transition from said third level of said programming transistor gate voltage back to said first level of said programming transistor gate voltage, and after said eighth transition, said

first circuitry causes a ninth transition from said first level of said programming voltage back to said second level of said programming voltage, and said second circuitry causes a tenth transition from said first level of said programming transistor gate voltage to a fourth level of said programming transistor gate voltage close enough to said second level of said programming voltage to turn off said programming transistor.

[c15] 15. The circuit as recited in claim 6, wherein after said second transition, said first circuitry causes a third transition from said second level of said programming voltage back to said first level of said programming voltage, and said second circuitry causes a fourth transition from said second level of said programming transistor gate voltage back to said first level of said programming transistor gate voltage, and after said third transition, said first circuitry causes a fifth transition from said first level of said programming voltage to a third level of said programming voltage lower than said second level of said programming voltage and close enough to said bias voltage level that said switch would be turned off if said third level of said programming voltage were applied to said shared gate terminal of said switch, and said second circuitry causes a sixth transition from said first level of said programming transistor gate voltage to a third level

of said programming transistor gate voltage greater than said third level of said programming voltage, whereby said programming transistor is turned off.

[c16] 16. The circuit as recited in claim 6, further comprising a third circuit for turning off said switch, said third circuit comprising a transistor having its drain connected to said shared gate terminal of said switch and having its source connected to said connected sources of said switch.

[c17] 17. The circuit as recited in claim 6, further comprising:
a plurality of ultrasound transducers;
a driving circuit;
a receiver; and
a plurality of high-voltage switching circuits connected to said plurality of ultrasound transducers, wherein each of said switching circuits comprises a respective switch as recited in claim 6, said driving circuit or said receiver being coupled to any one of said ultrasound transducers by way of one or more of said switches.

[c18] 18. A circuit comprising:
a switch having ON and OFF states and having a parasitic gate capacitance, said switch comprising a pair of DMOS FETs having a shared gate terminal, the sources of said DMOS FETs being connected to each other and the drains

of said DMOS FETs being connected to the input and output terminals of said switch respectively;

a control circuit for turning said switch on and off, said control circuit comprising a first level shifter having an input terminal and an output terminal, and a programming transistor having its drain connected to said shared gate terminal of said switch, having its source connected to a first terminal from which said programming transistor draws current, and having its gate connected to receive a voltage derived from a voltage output by said first level shifter; and

a resistance connected across said switch output terminal and a second terminal,

wherein said switch turns on in response to the following conditions: a first gate control voltage level is applied to said input terminal of said first level shifter that results in said programming transistor passing current, while first and second bias voltage levels are respectively applied to said first and second terminals to produce a switch gate-source voltage that turns said switch on.

[c19] 19. The circuit as recited in claim 18, wherein said control circuit further comprises:

a second level shifter having an input terminal and an output terminal; and

floating control logic having an output terminal con-

nected to said gate of said programming transistor and having first and second input terminals respectively connected to said output terminals of said first and second level shifters, the voltage level applied to said gate of said programming transistor being a function of the inputs to said floating control logic,
wherein said switch turns off in response to the following conditions: a second gate control voltage level is applied to said input terminal of said second level shifter that results in said programming transistor passing current, while third and fourth bias voltage levels are respectively applied to said first and second terminals to produce a switch gate-source voltage that turns said switch off.

[c20] 20. The circuit as recited in claim 19, wherein said first bias voltage level is greater than said third bias voltage level, while said second and fourth bias voltage levels are equal to each other.

[c21] 21. The circuit as recited in claim 18, wherein said programming transistor is a PMOS transistor.

[c22] 22. The circuit as recited in claim 21, wherein said PMOS transistor comprises a body, the body and the source of said PMOS transistor being shorted.

[c23] 23. The circuit as recited in claim 21, wherein said PMOS transistor comprises a body disconnected from the source of said PMOS transistor and tied to a bias voltage different than the voltage applied at said source of said PMOS transistor.

[c24] 24. The circuit as recited in claim 21, wherein said drain of said PMOS transistor is connected to said shared gate terminal of said switch without an intervening diode.

[c25] 25. The circuit as recited in claim 18, further comprising a turn-off circuit comprising:
a second level shifter having an input terminal and an output terminal; and
a gate clamp transistor having its drain connected to said shared gate terminal of said switch, its source connected to a junction of the sources of said DMOS FETs and to said second level shifter, and its gate connected to said second level shifter,
wherein said switch turns off in response to the following conditions: a second gate control voltage is applied to said input terminal of said second level shifter that results in said gate clamp transistor passing current, which has the effect of shorting said shared gate terminal of said switch to said shared source terminal of said switch.

[c26] 26. The circuit as recited in claim 18, further comprising

an ultrasound transducer coupled to said output terminal of said switch and driven by said driver circuit when said switch and said driver circuit are both turned on.

[c27] 27. The circuit as recited in claim 26, further comprising a programming circuit for changing the voltage applied at said first terminal to a first voltage level when said driver circuit is activated, a second voltage level for turning said switch on, and a third voltage level for turning said switch off, wherein said first voltage level is higher than said second voltage level, and said second voltage level is higher than said third voltage level.

[c28] 28. The circuit as recited in claim 18, wherein said resistance is provided by a MOSFET having its drain connected to said switch output terminal and its source connected to said second terminal, the gate of said MOSFET being connected to a third terminal.

[c29] 29. The circuit as recited in claim 28, further comprising a programming circuit for changing the voltage applied at said third terminal to a first voltage level under a first condition of operation and a second voltage level under a second condition of operation.

[c30] 30. The circuit as recited in claim 18, further comprising: a plurality of ultrasound transducers;

an ultrasound transducer driving circuit; and
a plurality of high-voltage switching circuits respectively connected to said plurality of ultrasound transducers, wherein each of said switching circuits comprises a respective switch as recited in claim 17, each ultrasound transducer being coupled to a respective output terminal of a respective switch.

[c31] 31. A device comprising:
a first switch having ON and OFF states and having a parasitic gate capacitance, said first switch comprising a pair of DMOS FETs having a shared gate terminal, the sources of said DMOS FETs being connected to each other and the drains of said DMOS FETs being connected to the input and output terminals of said first switch respectively, and biased at a bias voltage level; and
a first control circuit for turning said first switch on and off, said first control circuit having first and second control states, each of said first and second control states being a function of a programming voltage and a programming gate voltage applied to different terminals of said first control circuit, wherein:
in said first control state of said first control circuit, said programming voltage has a first voltage level and said programming gate voltage has a voltage level less than said first voltage level, resulting in said first switch being

on; and

in said second control state of said first control circuit, said programming voltage has a second voltage level less than said first voltage level and said programming gate voltage has a voltage level less than said second voltage level, resulting in said first switch being off.

[c32] 32. The device as recited in claim 31, wherein said first control circuit also has third and fourth control states, wherein:

in said third control state of said first control circuit, said programming voltage has said first voltage level and said programming gate voltage has a voltage level approximately equal to said first voltage level, resulting in said first switch remaining off; and

in said fourth control state of said first control circuit, said programming voltage has said second voltage level and said programming gate voltage has a voltage level greater than said second voltage level, resulting in said first switch remaining on.

[c33] 33. The device as recited in claim 31, further comprising:

a driver circuit coupled to said input terminal of said first switch; and

a first ultrasound transducer coupled to said output terminal of said first switch,

wherein said driver circuit drives said first ultrasound

transducer with a drive voltage that is not greater than said programming gate voltage while said first control circuit is in said second control state.

[c34] 34. The device as recited in claim 33, further comprising a receiver circuit and a transmit/receive switch that selectively couples said driver and receiver circuits to said input terminal of said first switch.

[c35] 35. The device as recited in claim 31, wherein said control circuit comprises a PMOS transistor having its drain coupled to said gate terminal of said first switch, its source coupled to a terminal that receives said programming voltage, and its gate coupled to a terminal that receives said programming gate voltage.

[c36] 36. The device as recited in claim 35, further comprising a level shifter coupled to said gate of said PMOS transistor.

[c37] 37. The device as recited in claim 36, further comprising floating control logic disposed between said level shifter and said gate of said PMOS transistor.

[c38] 38. The device as recited in claim 36, further comprising non-floating control logic, wherein said level shifter is disposed between said non-floating logic and said gate of said PMOS transistor.

[c39] 39. The device as recited in claim 31, further comprising:
a second switch having ON and OFF states and having a parasitic gate capacitance, said second switch comprising a pair of DMOS FETs having a shared gate terminal, the sources of said DMOS FETs being connected to each other and the drains of said DMOS FETs being connected to the input and output terminals of said second switch respectively, and biased at a bias voltage level; and
a second control circuit for turning said second switch on and off, said second control circuit having first and second control states, each of said first and second control states being a function of a programming voltage and a programming gate voltage applied to different terminals of said second control circuit, wherein:
in said first control state of said second control circuit, said programming voltage has a third voltage level and said programming gate voltage has a voltage level less than said third voltage level, resulting in said second switch being on; and
in said second control state of said second control circuit, said programming voltage has a fourth voltage level less than said third voltage level and said programming gate voltage has a voltage level less than said fourth voltage level, resulting in said second switch being off, wherein said first voltage level of said programming

voltage causes said first switch to have a first resistance when said first switch is turned on, and said third voltage level of said programming voltage causes said second switch to have a second resistance different than said first resistance when said second switch is turned on40. The device as recited in claim 31, wherein said first switch comprises a pair of DMOS FETs having a shared gate terminal, the sources of said DMOS FETs being connected to each other and the drains of said DMOS FETs being connected to said input and output terminals of said first switch respectively, and the sources of said DMOS FETs being biased at a bias voltage approximately equal to said third gate voltage.

[c40] 4140. A method of operating a high-voltage switching circuit, comprising the following steps:
programming a first ON resistance value for said high-voltage switching circuit under a first set of operating conditions, comprising a first value for a predetermined parameter, by applying a first programming voltage to a gate of said high-voltage switching circuit;
determining that said parameter has changed from said first value to a second value under a second set of operating conditions; and
programming a second ON resistance value for said high-voltage switching circuit under said second set of

operating conditions by applying a second programming voltage different than said first programming voltage to said gate.

[c41] 41. A method for programming high-voltage switching circuits, comprising the following steps:

(a) manufacturing first and second high-voltage switching circuits;

(b) determining a first gate-source voltage that causes said first high-voltage switching circuit to have a desired ON resistance;

(c) determining a second gate-source voltage that causes said second high-voltage switching circuit to have said desired ON resistance, said first and second gate-source voltages being different;

(d) programming a control circuit to provide a first gate voltage to said first high-voltage switching circuit, said first gate voltage being dependent on the results of step (b); and

(e) programming said control circuit to provide a second gate voltage to said second high-voltage switching circuit, said second gate voltage being dependent on the results of step (c),

wherein said first and second gate voltages are different but produce approximately the same ON resistances during operation of said first and second high-voltage

switching circuits.